Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

Fabrication of plasmonic modulator on a SOI platform

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List of Partners concerned

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Executive Summary

This document shall incorporate (all) rules procedures concerning the technical and administrative management of the project and is therefore to be updated on a regular basis. Please look at www.navolchi.eu regularly for the latest version.

Change Records

Version	Date	Changes	Author
0.1 (draft)	2012-01-26	Start	Argishti Melikyan
1 (submission)	2012-01-31		

Introduction

The fabrication of plasmonic phase modulator has been successfully carried out by IMEC and KIT, by separating the entire fabrication process flow into three steps

- Mask design for the fabrication of silicon/plasmonic platform
- Fabrication of passive silicon on insulator (SOI) chips at IMEC
- Fabrication of active plasmonic parts at KIT

Mask design for the fabrication of silicon/plasmonic platform.

KIT has designed a mask for the fabrication of the passive silicon platform, which will be used for farther post-processing in order to define the plasmonic modulators. The essential parts of the mask are the silicon taper pairs with various separations from 2 μm to 45 μm, see Fig. 1. The silicon tapers have tapering angle of 15˚ and tip size of 120 nm, see **Milestone 25** "*Decision on optimized plasmonic waveguide couplers*".

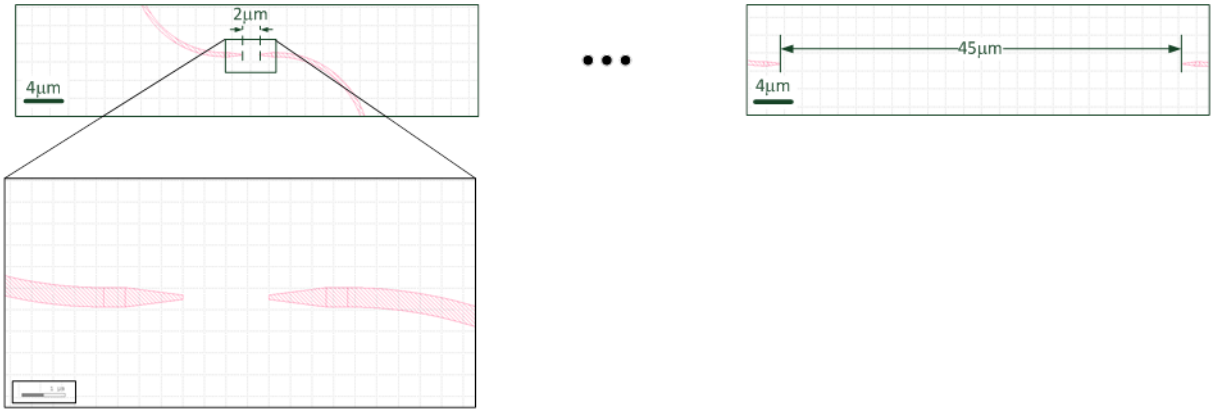

Figure 1 Silicon tapers designed for the fabrication of plasmonic modulator.

Fabrication of passive silicon on insulator (SOI) chips (IMEC)

IMEC has processed SOI wafer with a buried oxide and the silicon device layer thicknesses of 2 μm and 220 nm, respectively. KIT's designed mask layout with the size of 3 × 3mm has been exposed 30 times with various doses. Silicon nanowires with a width of 450nm and height of 220nm have been structured in HBr dry etching process. Standard diffraction grating couplers with a period of 625 nm and fill factor of 50 % have been design on the chip for light coupling in and out from the chip.

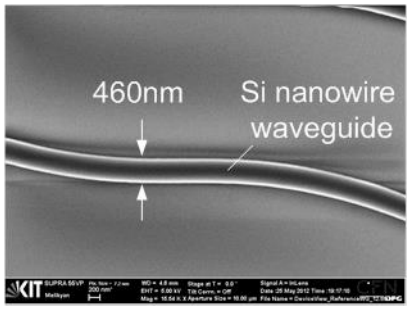

Figure 2 Scanning electron microscope picture of the fabricated silicon nanowire waveguide.

Silicon tapers with tapering angle of 15˚ and tip size of 120nm have been fabricated in the final etch step, see Fig. 2.

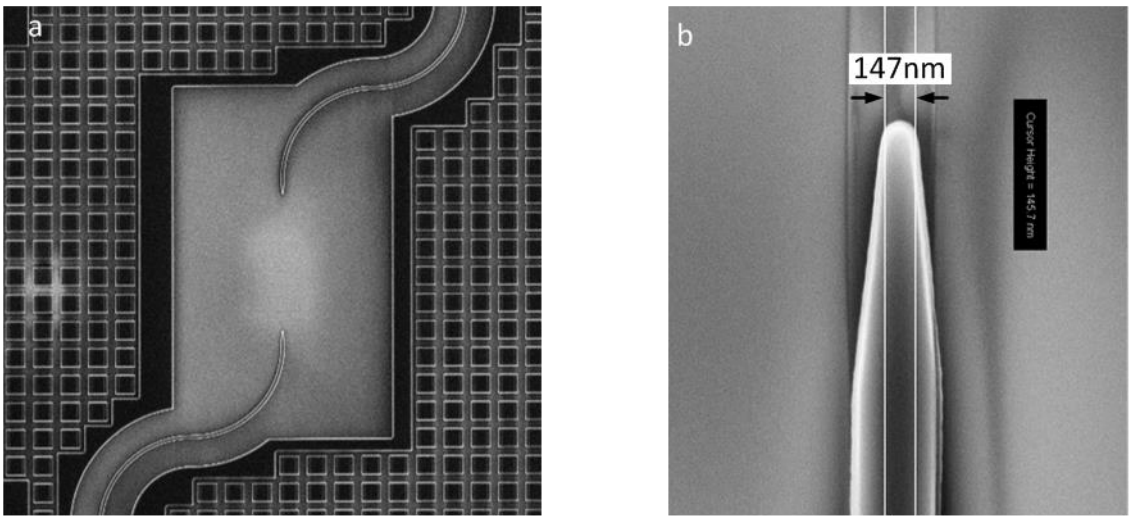

Figure 3 Fabricated passive silicon platform. (a) Fabricated the pair silicon tapers which will be used for light coupling in and out from the plasmonic modulator. (b) Fabricated silicon taper. Designed tip size of 120nm resulted in 150nm tip size.

Fabrication of active plasmonic parts (KIT)

The next step of the fabrication has been carried out at KIT employing e-beam lithography and lift-off techniques. 12 devices with various lengths have been exposed, and150nm of gold has been electron beam evaporated on the samples. The optical microscope picture of an array of the modulators is given in Fig. 4. The big metal electrodes with the dimensions of 150 × 130μm^2 are used as contact pads for GS RF probe.

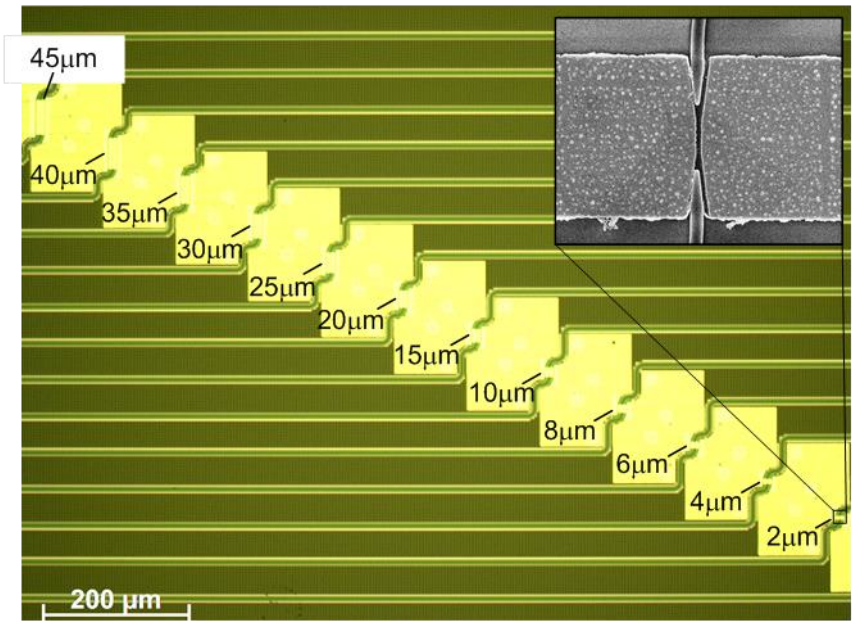

Figure 4 The array of fabricated plasmonic modulators with various length from 2μm to 45μm. Electrodes with a dimensions of 150 × 130μm^2 are used as contact pads.

Fabricated metal slot width is 140nm with slight variation with the device length. In Fig. 5 we give the scanning electron microscope pictures of fabricated device with a slot width of 140nm. It can be seen that fairly good fabrication alignment is achieved relative to the passive silicon platform fabricated by IMEC, see Fig. 5(b).

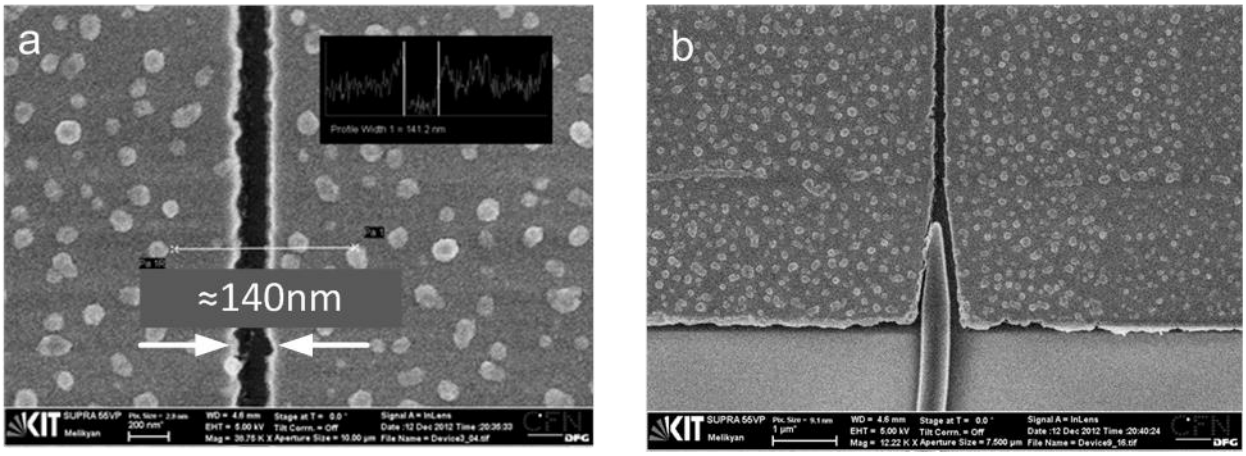

Figure 5 Fabricated metal slot and the interface with the silicon photonics. (a) fabricated plasmonic slot with width of 140nm. (b) metal taper mode converter used for light coupling in a and out from the plasmonic modulator

In the final step of the fabrication, the samples have been coated with commercially available nonlinear polymer M3 having a linear electro-optic coefficient of 70pm/V.